

Abstract

It is an object to, in a data storage circuit for storing data, provide a power saving data storage circuit
5 and a data writing method in the data storage circuit, and further, a data storage device.

Thus, in the present invention, reading out of existing data stored in a storage element M is performed prior to performing writing of new data to the storage
10 element M to compare the existing data and the new data. The data storage circuit is configured so that in a case where the existing data and the new data are identical with each other, writing to the storage element M is not performed and, in a case where the existing data and the
15 new data are not identical with each other, writing of the new data to the storage element M is performed. The data storage circuit is formed on a semiconductor substrate to have a data storage device.

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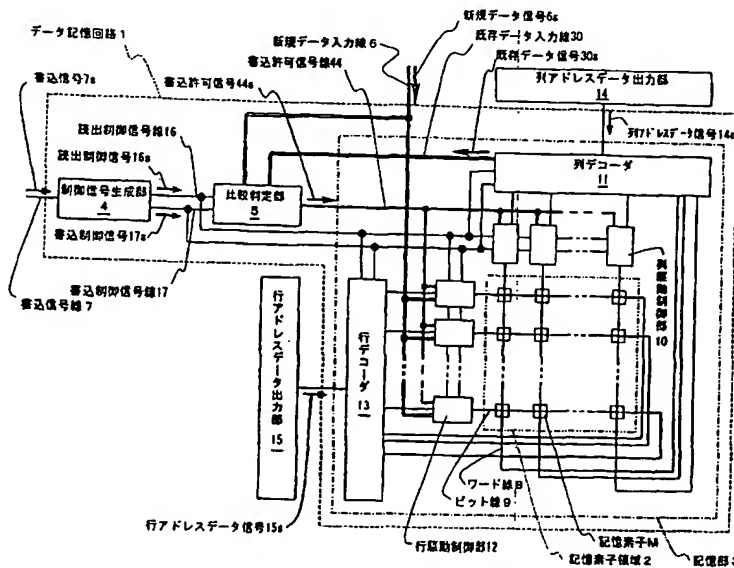
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(54) Title: DATA STORAGE CIRCUIT, DATA WRITE METHOD IN THE DATA STORAGE CIRCUIT, AND DATA STORAGE DEVICE

(54) 発明の名称: データ記憶回路及び同データ記憶回路におけるデータ書き込み方法及びデータ記憶装置



(57) Abstract: A data storage circuit for storing data and saving power. A data write method in the data storage circuit and a data storage device are also disclosed. Before writing new data in a storage element (M), existing data stored in the storage element (M) is read in and the existing data is compared to the new data. The data storage circuit is configured as follows. When the existing data coincides with the new data, no write is performed to the storage element (M). When the existing data does not coincide with the new data, the new data is written into the storage element (M). The data storage circuit is formed on a semiconductor substrate, so as to serve as a data storage device.

- 1...DATA STORAGE CIRCUIT
7s...WRITE SIGNAL
44s...WRITE ALLOW SIGNAL
44...WRITE ALLOW SIGNAL
6...NEW DATA INPUT LINE
6s...NEW DATA SIGNAL
30s...EXISTING DATA INPUT LINE
30s...EXISTING DATA SIGNAL
14...COLUMN ADDRESS DATA OUTPUT UNIT
14s...COLUMN ADDRESS DATA SIGNAL
11...COLUMN DECODER
16...READ OUT CONTROL SIGNAL LINE
16s...READ OUT CONTROL SIGNAL
4...CONTROL SIGNAL GENERATION UNIT
- 5...COMPARISON JUDGMENT UNIT
17s...WRITE IN CONTROL SIGNAL
17...WRITE IN CONTROL SIGNAL LINE
7...WRITE IN SIGNAL LINE
15...ROW ADDRESS DATA OUTPUT UNIT
13...ROW DECODER
8...WORD LINE
9...BIT LINE
15s...ROW ADDRESS DATA SIGNAL
12...ROW DRIVE CONTROL UNIT
2...STORAGE ELEMENT REGION
M...STORAGE ELEMENT
3...STORAGE UNIT
10...COLUMB DRIVE CONTROL UNIT

(57) 要約: データの記憶を行なうデータ記憶回路において、省電力化したデータ記憶回路及び同データ記憶回路におけるデータ書き込み方法、さらにデータ記憶装置を提供することを課題とする。そこで本発明では、記憶素子Mに新規データの書き込みを行なう前に、同記憶素子Mが記憶している既存データの読み込みを行ない、既存データと新規データとを比較して、既存データと新規データとが一致する場合には記憶素子Mへの書き込みを行わず、既存データと新規データとが不一致の場合には

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